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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/774,990	AMATANGELO ET AL.	
	Examiner	Art Unit	
	Shambhavi Patel	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 July 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,8-10 and 16-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-10 and 16-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to the Amendments/Remarks submitted 09 July 2007.

2. Claims 1-6, 8-10 and 16-20 have been presented for examination.

Response to Arguments

3. In view of Applicant's amendments, the previously issued 35 U.S.C. 101 rejection of claim 1 and all 112 rejections are **withdrawn**. The Examiner notes that a **new 35 U.S.C. 112 rejection has been issued** below based on the newly amended limitations.

4. Applicant's arguments with respect to the 35 U.S.C. 102 rejection of claims 1-6, 8-10 and 16-20 have been considered but are **moot** in view of the new ground(s) of rejection.

5. Applicant's arguments filed 09 July 2007 regarding the 35 U.S.C. 101 rejection of claims 6 and 16 0 have been fully considered but they are **not persuasive**.

Regarding the 35 U.S.C. 101 rejection:

i. The Examiner respectfully asserts that regarding **claim 6**, classifying a combinatorial gate as a clock gate or a near domino gate is not a tangible result.

ii. **Applicant submits**, on page 5 of the remarks, that **claim 16** is statutory because it is directed to a structure. **The Examiner** notes that it is unclear what statutory category the claim is directed to. Furthermore, given its broadest reasonable interpretation, the "structure" of claim 16 can be interpreted as being comprised solely of software elements, and is therefore nonstatutory.

Claim Objections

6. **Claims 8-10** are objected to for depending from cancelled claims. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. **Claims 1-6, 8-10 and 16-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite** for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Regarding **claim 1**, the limitations "...when the output of the combinatorial gate feeds into a clock input of a sequential circuit" and "when the output of the combinatorial gate feeds into the input of a dynamic circuit" are indefinite. It is unclear where in the claim it is determined what the output of the combinatorial gate feeds into. When is the detection done? Does it happen automatically after the signal has been propagated to the input? Is it done before the propagation? The limitation "providing a static timing model of the combinatorial gate" is indefinite. Based on the claim, it is unclear how the model is formed. Regarding **claim 6**, the limitations "...when the output of the combinatorial gate feeds into a clock input of a sequential circuit" and "when the output of the combinatorial gate feeds into the input of a dynamic circuit" are indefinite. It is unclear where in the claim it is determined what the output of the combinatorial gate feeds into. When is the detection done? Does it happen automatically after the signal has been propagated to the input? Is it done before the propagation? The term "classifying" is indefinite.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

8. **Claims 6, 8-10 and 16-20 are rejected under 35 U.S.C. 101** because the claimed invention is directed to non-statutory subject matter. The Examiner asserts that the current state of the claim language is such that a reasonable interpretation of the claims would not result in any useful, concrete or tangible product. **Claim 6** is directed to a method of determining how to model a combinatorial gate where the

combinatorial gate receives a data signal and a clock signal. **Claim 16** is directed to a static time engine. This claimed subject matter lacks a practical application of a judicial exception (law of nature, abstract idea, naturally occurring article/phenomenon) since it fails to produce a useful, concrete and tangible result. Specifically, the claimed subject matter does not produce a tangible result because the claimed subject matter fails to produce a result that is limited to having real world value rather than a result that may be interpreted to be abstract in nature as, for example, a thought, a computation, or manipulated data. More specifically, the claimed subject matter provides for propagating/modeling the data signal as an output when the output of the combinatorial gate corresponds to a data signal **(claim 6)**, and means for modeling the output of the combinatorial gate as a data signal **(claim 16)**. These produced results remain in the abstract and, thus, fail to achieve the required status of having real world values. **Claim 16** is not statutory because it is software, per se. Given its broadest, most reasonable interpretation, the static engine in claim 16 (interpreted in light of pages 9-10 of the specification) is comprised solely of software modules. All other claims are rejected by virtue of dependency.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. **Claims 1, 3 and 4 are rejected under 35 U.S.C. 102(b)** as being clearly anticipated by **Wang (US Patent No. 5,579,510).**

Regarding claim 1:

Wang discloses a computer-implemented method of modeling the static timing behavior of a combinatorial gate comprising:

a. determining that a data signal has been propagated to a first input of the combinatorial gate **(column 11 lines 24-34 "the second input terminal of the OR-gate is driven by a data signal")**

b. determining that a clock signal has been propagated to a second input of the combinatorial gate **(column 11 lines 24-34 "the first input terminal of the OR-gate is driven by a clock signal")**

c. propagating the clock signal as an output signal of the combinatorial gate when the output of the combinatorial gate feeds into a clock input of a sequential circuit **(column 11 lines 29-34 "gated-clock")**

d. propagating the data signal as an output signal of the combinatorial gate when the output of the combinatorial gate feeds into a data input of a dynamic circuit **(column 11 lines 24-34 "clocked-gate")**

e. providing a static timing model of the combinatorial gate **(abstract)**

Regarding claim 3:

Wang discloses the method of claim 1 propagating the data signal includes includes causing a later arriving edge of the data signal to cause the output signal to respond **(column 6 lines 26-44)**

Regarding claim 4:

Wang discloses the method of claim 1 wherein: the data signal includes a single edge per clock period; and, when propagating the data signal, the single edge is propagated through the combinatorial gate **(column 12 lines 61-67; column 13 lines 1-7)**.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

10. Claim(s) 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Wang (US Patent No. 5,579,510).**

Regarding claim 5:

Wang does not explicitly disclose the method of claim 1 wherein: the clock signal includes two edges per clock period; and, when propagating the clock signal, the two edges are propagated through the combinatorial gate. However, Wang teaches, that as is common in synchronous circuits, the clock waveform has a known phase relationship **(column 10 lines 56-56).** Thus, if the number of edges per

period is known, a skilled artisan would obviously pass through all the edges in order to prevent outputting a distorted clock signal.

11. Claim(s) 2, 6 and 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Wang (US Patent No. 5,579,510) in view of Zhao ("Timing-Driven Partitioning and Timing Optimization of Mixed Static-Domino Implementations",** 2000).

Regarding claim 2:

Wang does not explicitly disclose the method of claim 1 further comprising performing a reverse traversal function on a circuit design containing the combinatorial gate. **Zhao teaches** performing reverse traversals on circuit designs containing both static and domino circuits **(Zhao: page 1329 "Determining the Candidate Cut Nodes" reverse PERT traversal).** At the time of the invention, it would have been obvious to one of ordinary skill in the art to combine the teachings of Wang and Zhao because the methodology of Zhao minimizes implementation costs while meeting timing constraints **(Zhao: section III page 1332 left column 2nd complete paragraph).**

Regarding claim 6:

Wang discloses a method of determining how to model a combinatorial gate where the combinatorial gate receives a data signal and a clock signal comprising:

a. classifying the combinatorial gate as a clock gate when the output of the combinatorial gate is tied to a clock input of a sequential circuit **(column 11 lines 29-34 "gated-clock")**
b. classifying the combinatorial gate as a near domino gate when the output of the combinatorial gate is tied to a data input of a dynamic circuit **(column 11 lines 24-34 "clocked-gate")**.

Wang does not explicitly disclose performing a reverse traversal. **Zhao teaches** performing reverse traversals on circuit designs containing both static and domino circuits **(Zhao: page 1329 "Determining the Candidate Cut Nodes" reverse PERT traversal).** At the time of the invention, it would have been obvious to one of ordinary skill in the art to combine the teachings of Wang and Zhao because the methodology of Zhao minimizes implementation costs while meeting timing constraints **(Zhao: section III page 1332 left column 2nd complete paragraph).**

Regarding claim 8:

Wang discloses the method of claim 6 wherein classifying the combinatorial gate as a near domino gate further comprises causing a later arriving edge of the data signal to cause the output signal to respond **(column 6 lines 26-44)**

Regarding claim 9:

Wang discloses the method of claim 6 wherein: the data signal includes a single edge per clock period; and, when classifying the combinatorial gate as a near domino gate, the single edge is propagated through the combinatorial gate **(column 12 lines 61-67; column 13 lines 1-7).**

Regarding claim 10:

Wang does not explicitly disclose the method of claim 6 wherein: the clock signal includes two edges per clock period; and, when propagating the clock signal, the two edges are propagated through the combinatorial gate. However, Wang teaches, that as is common in synchronous circuits, the clock waveform has a known phase relationship **(column 10 lines 56-56).** Thus, if the number of edges per period is known, a skilled artisan would obviously pass through all the edges in order to prevent outputting a distorted clock signal

12. Claim 16-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Rajsuman (US Patent No. 5,867,036) in view of Zhao ("Timing-Driven Partitioning and Timing Optimization of Mixed Static-Domino Implementations",** 2000**).**

Regarding claim 16:

Rajsuman discloses the static timing engine comprising:

a. a data model, the data model including a combinational block determinator module **(column 6 lines 32-38).**

b. timing engine portion coupled to the data model, the timing engine portion including means for modeling an output of the combinatorial gate as a clock signal when an input to a next element of the circuit is clock input; and, means for modeling the output of the combinatorial gate as a data signal when an input to a next element of the circuit is a data input **(column 7 lines 11-23).** When the domino clock is 0, the domino logic is being initialized, and the output is 0 (equivalent to the clock input). When the domino clock is 1, the evaluation phase is entered, and the test vector (data input) is applied to the domino logic and the response (output) is stored in the register.

Rajsuman does not explicitly disclose the method of claim 1 further comprising performing a reverse traversal function on a circuit design containing the combinatorial gate. **Zhao teaches** performing reverse traversals on circuit designs containing both static and domino circuits **(Zhao: page 1329 "Determining the Candidate Cut Nodes" reverse PERT traversal).** At the time of the invention, it would have been obvious to one of ordinary skill in the art to combine the teachings of Rajsuman and

Zhao because the methodology of Zhao minimizes implementation costs while meeting timing constraints **(Zhao: section III page 1332 left column 2nd complete paragraph).**

Regarding claim 17:

Rajsuman discloses the static timing engine of claim 16 wherein: the means for modeling the output of the combinatorial gate as a data signal includes means for modeling a near domino function **(column 7 lines 11-23).**

Regarding claim 18:

Rajsuman discloses the static timing engine of claim 17 wherein: the near domino function includes causing a later arriving edge of the data signal to cause the output signal to respond **(column 6 lines 2-6).**

Regarding claim 19:

Rajsuman discloses the static timing engine of claim 17 wherein: the data signal includes a single edge per clock period; and, when providing the near domino function, the single edge is propagated through the combinatorial gate **(column 6 lines 54-59).**

Regarding claim 20:

Rajsuman discloses the static timing engine of claim 17 wherein: the clock signal includes two edges per clock period; and, when propagating the clock signal, the two edges are propagated through the combinatorial gate **(column 7 lines 2-10).** The minimum period that the clock can be low for can be selected, and thus if the clock has two low edges during the period, both edges will be propagated through.

Conclusion

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

14. **Examiner's Remarks:** Examiner has cited particular columns and line numbers in the references applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in their entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner. In the case of amending the claimed invention, Applicant is respectfully requested to indicate the portion(s) of the specification which dictate(s) the structure relied on for proper interpretation and also to verify and ascertain the metes and bounds of the claimed invention.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shambhavi Patel whose telephone number is (571) 272-5877. The examiner can normally be reached on Monday-Friday, 8:00 am – 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on (571) 272-2279. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SKP

KAMINI SHAH
SUPERVISORY PATENT EXAMINER